

GEANT P4 lab (aka GP4L)

Carmen MISA MOREIRA CERN – RARE project participant carmen.misa.moreira@cern.ch

TNC22 June 15th 2022 Public



Agenda

- GÉANT-4 Programme
- GP4L Mission statement
- A bit of context ...
 - Programming Protocol-independent Packet Processors: P4 language
 - Network Operating System
 - P4 Programmable Switches: EdgeCore Wedge100BF-32QS
- GP4L GÉANT P4 LAB footprint
- GP4L Use case at CERN
- How can you benefit from GP4L ?

GÉANT-4 Programme

39 participants country

- NREN participants
- But also NREN staff members !

GN4 phase 3 cooperation programme

- 44 months
- Budget 78 M€

GN4-3 divided in "Work Package"

- 9 WP divided in "Tasks"
- Task 1 encompasses 6 Sub-tasks
- RARE/GP4L within a sub-task

GP4L Mission statement

- Primarily used to validate the software code inherently part of <u>RARE/freeRtr</u> open source routing stack.
- It is a service that is under development with the aim to provide experimental dataplane programming facilities where researchers can elaborate and test representative and geographically distributed network experiment
 - With the usage of <u>RARE/freeRtr</u> Operating System
 - Or simply use a clean slate environment.

(i.e use exclusively **GP4L** without <u>RARE/freeRtr</u> dataplane & control plane)



A bit of context...

P4 language, Network Operating System and P4 Programmable Switches



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A bit of context...

Programming Protocol-independent Packet Processors: P4 language

Language for programming the data plane of network devices

- Define how packets are processed
- P4 program structure: header types, parser/deparser, match-action tables, user-dened metadata and intrinsic metadata

Domain-specific language designed to be implementable on a large variety of targets

• Programmable network interface cards, FPGAs, software switches and hardware ASICs.

A bit of context... Network Operating System

RARE/FreeRtr

- Controls the data plane by managing entries in routing tables
- Free and open source router operating system
- Export forwarding tables to DPDK or hardware switches
 - via OpenFlow or P4lang
- No global routing table
- Every routed interface must be in a virtual routing table









A bit of context... P4 Programmable Switches

EdgeCore Wedge100BF-32QS:

100GbE Data Center Switch

- Bare-Metal Hardware
- L2/L3 Switching
- 32xQSFP28 Ports
- Data-Plane Programmability
 - Intel Tofino Switch Silicon
 - Barefoot Networks
- Quad-Pipe Programmable Packet Processing Pipeline
 - 6.4 Tbps Total Bandwidth
- CPU: Intelx86 Xeon 2.0GHz
 - 8-core/48GB/2TBSSD







GP4L GÉANT P4 LAB footprint



GP4L – GÉANT P4 LAB





GP4L – GÉANT P4 LAB: topology rendering via BGP-LS_[1]



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GP4L – GÉANT P4 LAB



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GP4L Use case at CERN



Packet Marking Specification: IPv6 Flow Label

Research Network Technology WG proposed a packet marking technique to identify the LHC experiment and the application that has generated a transmission packet [1]

- The Experiment-Application tag is inserted in the flow label field of the IPv6 packet header.
- The original purpose of the field was never implemented, so it has been neglected by most of the existing network devices.

Primary goal of the marking is to count the traffic, but special routing polices could also be applied.

DUNE

- 8192

Flow label field of IPv6 header: 20 bits

- 5 entropy bits to match RFC 6436
- 9 bits to define the science domain

• 6 bits to define the application/type of traffic



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Programmable Switches for Flow Label Accounting and Routing

Flow label is inserted transparently on LHCOPN link to a Tier1 The traffic is separated-counted-aggregated internally



Programmable Switches for Flow Label Accounting and Routing

Data transfers with flow label

Network configuration:

- Emulates a Tier 1/0 link
- Tier1/0 routers
 - IPv4/IPv6 BGP peerings
- Tier0 router
 - LHCOPN production border router
- Pure layer 2 bridges
 - VLAN 1000: IPv4 traffic
 - VLAN 1001: IPv6 traffic
- Tier0 servers
- OpenStack product servers





Programmable Switches for Flow Label Accounting and Routing

P4 switch network configuration: pure layer 2 bridges

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MultiONE multiple "LHCONEs": Traffic separation with IPv6 flow labels



Route the traffic of the different LHC experiments into the appropriate VPN.

• A prototype of a flow label router is being developed using a P4 programmable switch (EdgeCore Wedge100BF-32QS with Intel Tofino processor)



ExpB

Useful links



Project:

GP4L project page: <u>https://wiki.geant.org/display/GP4L/Home</u> RARE/freeRtr: <u>https://www.rare.freertr.net</u> <u>https://docs.freertr.net</u> <u>https://blog.freertr.net</u>

Contact:

Users: gp4l-users@lists.geant.org Developer wanabee: gp4l-dev@lists.geant.org Project: gp4l@lists.geant.org



Looking ahead: Finalize transition to production



Validate your use case with GP4L!

Orchestrate and automate GP4L:

Lab reservation Persistent testbed interaction at global scale

New hardware: TOFINO2 NVIDIA DPU

P4 SmartNIC TOFINO/FPGA

Global worldwide footprint:

Interconnection with other persistent testbed

➔ New idea:

Validate new use cases Scalability 100/400 GE DTN automation Control plane scalability



And more ...



Thank you

Any questions?

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© GÉANT Association on behalf of the GN4 Phase 3 project (GN4-3). The research leading to these results has received funding from the European Union's Horizon 2020 research and innovation programme under Grant Agreement No. 856726 (GN4-3).